IN THE CLAIMS:

Amend claims 23-25 and add 26-40 as follows:

1.(Cancelled)

2.(Cancelled)

3.(Cancelled)

4.(Cancelled)

5.(Cancelled)

6.(Cancelled)

7.(Cancelled)

8.(Cancelled)

9.(Cancelled)

10.(Cancelled)

11.(Cancelled)

12.(Cancelled)

13.(Cancelled)

14.(Cancelled)

15.(Cancelled)

16.(Cancelled)

17.(Cancelled)

18.(Cancelled)

19.(Cancelled)

20.(Cancelled)

21.(Cancelled)

22.(Cancelled)

23.(Currently Amended) A system for compensating for distortion within an analog-to-digital converter, the system comprising:

a test signal generator that provides an analog test signal and a digitized test signal indicative of the analog test signal;

an analog-to-digital converter that selectively receives an input signal and the analog test signal and provides a digitized signal;

a compensation circuit that receives the digitized signal and filter coefficients, and provides a compensated digitized signal;

a test signal check device that receives and processes the compensated digitized signal to extract a sequence of output data;

a difference unit that receives the sequence of output data and the compensated digitizeddigital signal and provides a difference signal indicative of the difference; and

a coefficient determination unit that receives the difference signal and the digitized signal and provides the filter coefficients.

24.(Currently Amended) A system for compensating for distortion within an analog-to-digital converter, the system comprising:

means for providing an analog test signal;

an analog-to-digital converter that selectively receives an input signal and the analog test signal and provides a digitized signal;

compensation means for receiving the digitized signal and adaptive filter coefficients, and for providing a compensated digitized signal;

means for receiving and processing the compensated digitized signal to extract a sequence of output data;

a difference unit that receives the sequence of output data and the compensated digitized ~~digital~~ signal and provides a difference signal indicative of the difference; and

means responsive to the difference signal and the digitized signal for providing the filter coefficients.

25.(Currently Amended) A system for compensating for distortion within an analog-to-digital converter, the system comprising:

a test signal generator that provides an analog test signal;

an analog-to-digital converter that selectively receives an input signal and the analog test signal and provides a digitized signal;

compensation means for receiving the digitized signal and filter coefficients, and for providing a compensated digitized signal;

means for receiving and processing the compensated digitized signal to extract a sequence of output data;

a difference unit that receives the sequence of output data and the compensated digitized ~~digital~~ signal and provides a difference signal indicative of the difference; and

means responsive to the difference signal and the digitized signal for providing the filter coefficients.

26. (New) The system of claim 23, where the compensation circuit comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$.

27. (New) The system of claim 23, where the compensation circuit comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$ where $m = \left\lfloor N \cdot \frac{x_n + 1}{2} \right\rfloor$.

28. (New) The system of claim 26, where the coefficients c_k are computed as a function of the digitized signal.

29. (New) The system of claim 23, where the test signal check device comprises a CORDIC unit responsive to in-phase and quadrature components of the digitized signal y_n to provide an amplitude signal to a DC component recovery circuit that provides the sequence of output data.

30. (New) The system of claim 23, further comprising a timing unit that selectively determines whether the input signal or the analog test signal is processed by the analog-to-digital converter.

31. (New) The system of claim 24, where the compensation circuit comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$.

32. (New) The system of claim 24, where the compensation circuit comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$ where $m = \left\lfloor N \cdot \frac{x_n + 1}{2} \right\rfloor$.

33. (New) The system of claim 31, where the coefficients c_k are computed as a function of the digitized signal.

34. (New) The system of claim 24, where the means for receiving and processing comprises a CORDIC unit responsive to in-phase and quadrature components of the digitized signal y_n to provide an amplitude signal to a DC component recovery circuit that provides the sequence of output data.

35. (New) The system of claim 24, further comprising a timing unit that selectively determines whether the input signal or the analog test signal is processed by the analog-to-digital converter.

36. (New) The system of claim 25, where the compensation means comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$.

37. (New) The system of claim 25, where the compensation means comprises a compensator unit that provides the compensated digitized signal y_n based upon the expression $y_n = \sum_{k=0}^{k} c_k(m) \cdot x_n^k$ where $m = \left\lfloor N \cdot \frac{x_n + 1}{2} \right\rfloor$.

38. (New) The system of claim 36, where the coefficients c_k are computed as a function of the digitized signal.

39. (New) The system of claim 25, where the means for receiving and processing comprises a CORDIC unit responsive to in-phase and quadrature components of the digitized signal y_n to provide an amplitude signal to a DC component recovery circuit that provides the sequence of output data.

40. (New) The system of claim 23, further comprising a timing unit that selectively determines whether the input signal or the analog test signal is processed by the analog-to-digital converter.